AMENDMENTS TO THE CLAIMS

This listing of Claims shall replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A timer circuit comprising:

an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and

a pull-down path coupled to said output stage and comprising a first circuit for providing a selectable amount of pull down current, wherein said plurality of selectively-activated components ~~comprise components different from~~ are of a different component type than components of said first circuit for providing a selectable amount of pull down current, said pull-down path ~~also coupled to receive~~ further comprising a second circuit for varying said delay through said timer circuit based upon temperature, wherein said second circuit is operable to vary said delay based upon a reference signal that ~~varies in proportion to temperature, and wherein said delay through said timer circuit~~ is inversely proportional to said temperature.

2. (Original) A timer circuit as described in Claim 1 wherein said reference signal is derived from a band gap reference circuit.

3. (Currently Amended) A timer circuit as described in Claim [[2]] 1, wherein ~~said reference signal is a VPTAT voltage signal~~ components of said second circuit are placed in a fixed state during manufacturing.

4. (Previously Presented) A timer circuit as described in Claim 1 wherein said plurality of selectively-activated components comprise a plurality of gated capacitors which can be selectively coupled to said output stage via a plurality of corresponding pass gates.

5. (Original) A timer circuit as described in Claim 4 wherein said configurable delay element further comprises a plurality of configuration bits each for controlling a respective pass gate.

6. (Currently Amended) A timer circuit as described in Claim 1, wherein said first circuit for providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled in parallel, and wherein each gated pull-down circuit comprises a first transistor having a gate controlled by a respective configuration bit and a series coupled second transistor having a gate controlled by said reference signal.

7. (Currently Amended) A timer circuit as described in Claim 4, wherein said first circuit for providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled in parallel, and wherein each gated pull-down circuit comprises a first transistor having a gate controlled by a

respective configuration bit and a series coupled second transistor having a gate controlled by said reference signal.

8. (Previously Presented) A timer circuit as described in Claim 6 wherein said plurality of selectively-activated components comprise a plurality of gated capacitors which can be selectively coupled to said output stage via a plurality of corresponding pass gates.

9. (Original) A timer circuit as described in Claim 8 wherein said configurable delay element further comprises a plurality of configuration bits each for controlling a respective pass gate.

10. (Currently Amended) An electronic device comprising a timer circuit and wherein said timer circuit comprises:

an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and

a pull-down path coupled to said output stage and comprising a circuit for providing a selectable amount of pull down current, wherein said plurality of selectively-activated components ~~comprise components different from~~ are of a different component type than components of said first circuit for providing a selectable amount of pull down current, said pull-down path ~~also coupled to receive~~ further comprising a second circuit for varying said delay through said timer circuit based upon temperature, wherein said second circuit is operable to

vary said delay based upon a reference signal that ~~varies in proportion to temperature, wherein said delay through said timer circuit~~ is inversely proportional to said temperature, and wherein said reference signal is derived from a band gap reference circuit.

11. (Original) An electronic device as described in Claim 10 wherein said reference signal is a VPTAT voltage signal.

12. (Previously Presented) An electronic device as described in Claim 10 wherein said plurality of selectively-activated components comprise a plurality of gated capacitors which can be selectively coupled to said output stage via a plurality of corresponding pass gates.

13. (Currently Amended) An electronic device as described in Claim 10, wherein said first circuit for providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled in parallel, wherein each gated pull-down circuit comprises a first transistor controlled by a respective configuration bit and a series coupled second transistor having a gate controlled by said reference signal.

14. (Previously Presented) An electronic device as described in Claim 13 wherein said plurality of selectively-activated components comprise a plurality of gated capacitors which can be selectively coupled to said output path via a plurality of corresponding pass gates.

15. (Original) An electronic device as described in Claim 10 wherein said electronic device is a memory circuit.

16. (Original) An electronic device as described in Claim 10 wherein said electronic device is a write back timer of a memory circuit.

17. (Currently Amended) A method of varying a delay of a timer circuit comprising:

during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit;

during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage; and

during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said varying ~~of~~ said delay of said timer circuit comprises varying said delay inversely proportional to a temperature of said timer circuit.

18. (Original) A method as described in Claim 17 wherein said reference signal is generated by a band gap circuit and varies proportionally with said temperature.

19. (Original) A method as described in Claim 18 wherein said pull down path comprises a plurality of parallel coupled pull down circuits, each pull down circuit comprising a first transistor coupled to a respective configuration bit of said second set of configuration bits and a second transistor having a gate coupled to said reference signal.

20. (Original) A method as described in Claim 19 wherein said elements are gated capacitors which can be selectively coupled to said output stage based on said first set of configuration bits.